IN THE SPECIFICATION

Please amend the specification as follows:

[0025] Preferably, provision is made of a chip (not shown) for processing the signal output through the signal line.

[0032] Further, there are the advantages that there is no need for charging including also the floating node capacity via the reset transistor, the increase of the driver size of the drain ~~lien~~ line can be prevented, and high speed operation can be secured.

[0034] [FIG. 2] A circuit diagram showing an example of the configuration of ~~for example~~ an MOS type solid state imaging device according to an embodiment of the present invention.

[0037] By the horizontal scanning pulses H being given and the turning on of the horizontal selection switch 33, the signal correlated double sampled (CDS) at the sample and hold/CDS circuit 31 is read out through the horizontal selection switch 33 to the horizontal signal line 32.

This read signal Hsig is derived from an output terminal 36 as an output signal Vout through an output amplifier [[35]] 38 connected to one end of the horizontal signal line [[35]] 32.

[0041] 10 . . . unit pixel, 11 . . . photodiode, 12 . . . transfer transistor, 13 . . . amplifier transistor, 14 . . . reset transistor, 22 . . . vertical signal line, 23 . . . drain line, 24 . . . reset line, 25 . . . V-shift register, 26 . . . P-type MOS transistor, 31 . . . sample & hold/CDS circuit, 32 . . . horizontal signal line, 34 . . . H shift register, 40 … camera system, 41 … imaging device, 42 … lens, 43 … drive circuit, 100 … unit pixel, 101 … photodiode, 102 … transistor, 103 … amplifier transistor, 104 … reset transistor, 105 … drain line, N101 … floating node.

[0043] FIG. 2 is a circuit diagram showing an example of the configuration of ~~for example~~ an MOS type solid state imaging device according to an embodiment of the present invention. Note that, in the MOS type solid state imaging device, a large number of unit pixels are arrayed in a matrix, but here, for simplification of the drawing, a pixel array comprised of two rows and two columns is drawn.

[0052] In the present embodiment, by driving the reset transistor 14 by three values (or four values or more) through the drain line 23, the V-shift register 25 provides a potential difference between potentials of the floating nodes ~~ND11~~ N11 in the selected row and the nonselected row and clarifies the operations in the two selected row and nonselected row.

[0071] FIGS. 3(A) to 3(G) and FIGS. 4(A) to 4(G) are diagrams indicating gate potentials (RST lines) V24 of the reset transistors and gate potentials (TR lines) V21 of

the transfer transistors 12 in the selected row and the nonselected row, a common drain power source potential V23, and a floating node potential ~~N11~~ VN11 in the case of operation by two values of the gate voltage of the reset transistor of VRST+ (plus side) and VRST- (minus side).

[0087] In comparison with the amplitude of the gate of the conventional reset transistor (amplitudes of the power source potential and the ground potential), when using [[A]] a negative potential according to the above method, the amplitude thereof becomes large, therefore the amount of the charging and discharging of the circuit is large, so there is an apprehension that a load will be applied to each potential generation circuit (or power supply).

[0088] Further, for this reason, in the case of a circuit ~~internallt~~ internally generating a negative potential, it is necessary to make the charge supply capability larger by exactly the amount of the amplitude. For this reason, the chip size increases.

[0104] First, at the time of nonselection, the potential of the floating node ~~N1~~ N11 becomes 0.5V. At this time, a power supply voltage [[dd]] Vdd, for example 3.0V, is output as a reset voltage B1 from the V-shift register 25. The potential of the drain line 23 also becomes the power supply voltage Vdd.

[0112] In this nonselected state, the potential of the floating node N11 is not 0V, but 0.5V, therefore the leakage of electrons to the photodiode 11 through the transfer transistor 12 is prevented. Here, the potential of the floating node [[N1]] N11 becomes 0.5V because of the action of the P-type MOS transistor 26 connected between the reset voltage output end of the V-shift register 25 and the drain line 23.

[0119] The camera system 40 has an imaging device 41, an optical system for guiding incident light to the pixel area of this imaging device 41, for example a lens 42 for focusing [[he]] the incident light (imaging light) onto an imaging surface, a drive circuit 43 for driving the imaging device 41, a signal processing circuit 44 for processing the output signal of the imaging device 41, and so on.

[0122] In this way, according to the present camera system, by using the MOS type solid state imaging device according to the previously explained embodiment as the imaging device 41, the MOS type solid state imaging device can make the noise from the nonselected row small, can suppress the occurrence of the vertical stripes in the bright scene, does not have to perform charging including the floating node capacity via the reset transistor, can prevent the increase of the driver size of the drain line, and can secure high speed operation, therefore an ~~imaging~~ image having a high quality with small noise can be obtained with a small circuit scale and a low power consumption.